abandonment of this application, then such extensions of time are hereby petitioned

under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net

addition of claims) are hereby authorized to be charged to our Deposit Account No.

19-0036.

Amendments

In the Claims:

Please add the following new claims:

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49. (New) A method for generating an aligned vector from two source vectors for

single instruction multiple data (SIMD) processing, comprising the steps of:

　　(1)　loading a first source vector into a first register;

　　(2)　loading a second source vector into a second register;

　　(3)　reading a first plurality of elements from said first register and a second

plurality of elements from said second register; and

　　(4)　writing said first plurality of elements and said second plurality of

elements into a third register in a particular order to produce a target vector having a

plurality of elements aligned for SIMD processing.

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3 50. (New) The method as recited in claim 49, wherein said writing step

comprises:

writing even-numbered, lower elements of said first register to said third register;

and

writing sign bits of odd-numbered, lower elements of said first register to said

third register.

4 51. (New) The method as recited in claim 49, wherein said writing step

comprises:

writing even-numbered, upper elements of said first register to said third register;

and

writing sign bits of odd-numbered, upper elements of said first register to said

third register.

5 52. (New) A method for generating an ordered set of elements in a target vector

from elements in a first source vector and a second source vector for single instruction

multiple data (SIMD) vector processing, comprising the steps of:

(1)   loading the first source vector into a first register;

(2)   loading the second source vector into a second register;

(3)   selecting a first subset of elements from said first register, said first subset

comprising any one of the following groups of elements from the first source vector: odd

elements, even elements, lower elements and upper elements; and

(4)   selecting a second subset of elements from said second register, said second subset comprising any one of the following groups of elements from the second source vector: odd elements, even elements, lower elements and upper elements.

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53. (New) The method of claim 52, further comprising the step of:

(5)   writing said first and said second subset of elements into a third register to facilitate a particular SIMD vector processing operation, said first subset being written into any one of the following groups of elements in said third register: upper elements, odd elements, and odd elements in reverse order, and said second subset being written into any one of the following groups of elements in said third register: lower elements, even elements, and even elements in reverse order, wherein elements written into said third register comprise the target vector.

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